Claim 17. (original) The LCOS cell structure of claim 12, wherein the break protective layer is a dielectric.

REMARKS

Present Status of the Application

The Office Action rejected all presently-pending claims 1-17. Specifically, the Office Action rejected claims 1, 2, 5-8 and 12-14 under 35 U.S.C. 102(e), as being anticipated by Walker et al. (U.S. 6,275,277). The Office Action also rejected claims 1-17 under 35 U.S.C. 103(a) as being unpatentable over Applicant's Prior Art Fig. 2 (APA) in view of JP No. 9-174909. Applicant has amended claims 5, 9 and 15 to clarify the claim scope of the present invention. After entry of the foregoing amendments, claims 1-17 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Summary of Applicant's Invention

The Applicant's invention is directed to a backpanel structure of liquid crystal on silicon to prevent the patterned trace on the cell region from being damaged in a breaking process. More particularly, a break protective layer is arranged on an alignment layer over the routing/pad region of a substrate to protect the patterned trace arranged on the routing/pad region from being damaged in a breaking process.

Response to 35 U.S.C. 112 objection

The limitation "the patterned trace" in Claims 9 and 15 lacks antecedent basis for this limitation in the claim.

Applicant respectfully asserts that Claims 9 and 15 are respectively revised to dependent to Claims 8 and 14, so that the "the patterned trace" recited in Claims 9 and 15 has antecedent basis for this limitation in the claim.

Response to 35 U.S.C. 102 (e) rejection

Claims 1, 2, 5-8 and 12-14 are rejected under 35 U.S.C. 102(e), as being anticipated by Walker et al. (U.S. 6,275,277).

Applicant respectfully asserts that Walker is legally deficient for the purpose of anticipating claim 1 for at least the reason that Walker fails to disclose every claimed feature of the present invention. More specifically, Walker fails to disclose ***"a break protective layer, arranged on the alignment layer direct above the routing/pad region"*** as taught in Claims 1 and 5, and ***"a silicon back panel having a cell region and a routing/pad region, wherein the routing/pad region is arranged with a break protective layer"*** as taught in Claim 12.

The present invention provides a backpanel structure of liquid crystal on silicon. A break protective layer is arranged on an alignment layer ***direct above*** the routing/pad region of a substrate. Since the routing/pad region of a substrate is covered by the protective layer, the patterned trace arranged ***direct above*** the routing/pad region is protected to prevent from being damaged in the breaking process.

In the Office Action, Examiner asserts that the unlabeled layer, which is arranged on the alignment layer 135, and between the cross-over material 170 and the sealing material 150, is a break protective layer arranged over the routing/pad region 119. However, in the matter of fact, contrary to the Office's assertion, Walker does not disclose "a break protective layer arranged on the alignment layer over the routing/pad region". The unlabeled layer in Figs. 34 and 35 of

Walker is arranged on the alignment layer 135 and between the cross-over material 170 and the sealing material 150, but the unlabeled layer ***is not arranged direct above*** the offset portion 119. Moreover, ***the pattern of the unlabeled layer is the same as that of the liquid crystal material 310*** and it did not describe a material of the unlabeled layer in col. 16, lines 33-51, ***so that the unlabeled layer is liquid crystal material 310, rather than the break protective layer made of, for example photoresist or dielectric*** as taught in present invention. Therefore, Walker fails to disclose ***"a break protective layer, arranged on the alignment layer direct above the routing/pad region"*** as taught in Claims 1 and 5, and ***"a silicon back panel having a cell region and a routing/pad region, wherein the routing/pad region is arranged with a break protective layer"*** as taught in Claim 12.

For at least Walker fails to disclose each element of the claim under consideration, Applicants submit that Walker does not anticipate the present invention, as recited in claims 1, 5 and 12. Applicants, therefore, respectfully request that the rejection of claims 1, 5 and 12, and claims 2-4, 6-11 and 13-14 dependent therefrom under 35 U.S.C. 102(e) be withdrawn.

Response to 35 U.S.C. 103 (a) rejection

claims 1-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Prior Art Fig. 2 (APA) in view of JP No. 9-174909

Applicant respectfully asserts that Applicant's Prior Art Fig. 2 (APA) in view of JP No. 9-174909 is legally deficient for the purpose of anticipating claims 1, 5 and 12 for at least the reason that Applicant's Prior Art Fig. 2 (APA) in view of JP No. 9-174909 fails to disclose every claimed feature of the present invention. More specifically, Applicant's Prior Art Fig. 2 (APA) in view of JP No. 9-174909 fails to disclose ***"a break protective layer, arranged on the***

alignment layer direct above the routing/pad region" as taught in Claims 1 and 5, and ***"a silicon back panel having a cell region and a routing/pad region, wherein the routing/pad region is arranged with a break protective layer"*** as taught in Claim 12.

JP No. 9-174909 discloses a thermal head, wherein ***a protective layer 9 is formed between the connection part of a connection terminal 34*** connected with a drive IC 4 and the pressure contact part with a flexible substrate 7. ***The protective layer 9 is formed on the connection terminal 34*** by screen printing simultaneously with the formation of a glass material on the conductor part 3. By this constitution, even when a sealing material flows in the connection direction with the flexible substrate 7 by its viscosity, it is obstructed by the protective layer 9 to be prevented from going over the protective layer to be formed. Therefore, the flexible substrate 7 can be certainly connected in a pressure contact state. In other word, *the structure of JP No. 9-174909 is* ***a back-end structure during a package process***.

However, *the structure of Applicant's Prior Art* ***is a backpanel structure of liquid crystal on silicon before a package process***. It is obvious that ***the process stage of the structure of JP No. 9-174909 is different from that of the structure of the Applicant's Prior Art***. Further, the protective layer 9 of JP No. 9-174909 *is used for preventing the sealing material from flowing over the protective layer to be formed.* It is obvious that ***the object of the formation of the protective layer 9 of JP No. 9-174909 has no concern with the patterned trace of the routing/pad region be damaged in the breaking stage***. Therefore, *the person of skill in the art* ***lakes motives to arranging the protective layer 9 of a back-end structure during a package process on the alignment layer direct above the routing/pad region before the package process***. Applicant's Prior Art Fig. 2 (APA) in view of JP No. 9-174909 fails to disclose ***"a break protective layer, arranged on the alignment layer direct above the routing/pad region"*** as

taught in Claims 1 and 5, and ***"a silicon back panel having a cell region and a routing/pad region, wherein the routing/pad*** region is arranged with a break protective layer" as taught in Claim 12.

On the other hand, if the Applicant's Prior Art combines with JP No. 9-174909, the final structure after combination is ***a backpanel structure of liquid crystal on silicon*** after breaking stage of the Applicant's Prior Art ***combines with the back-end structure*** of JP No. 9-174909 ***during a package process***. That is, ***the backpanel structure is connected with a drive IC 4, the drive IC 4 is connected with connection terminal 34, and protective layer 9 is formed between the connection part of a connection terminal 34 and the pressure contact part with a flexible substrate 7 to prevent the sealing material from flowing over the protective layer to be formed.*** Accordingly, the final structure of the Applicant's Prior Art combined with JP No. 9-174909 is different form this invention. Applicant's Prior Art Fig. 2 (APA) in view of JP No. 9-174909 fails to disclose ***"a break protective layer, arranged on the alignment layer direct above the routing/pad region"*** as taught in Claims 1 and 5, and ***"a silicon back panel having a cell region and a routing/pad region, wherein the routing/pad*** region is arranged with a break protective layer" as taught in Claim 12.

For at least Applicant's Prior Art Fig. 2 (APA) in view of JP No. 9-174909 fails to disclose each element of the claim under consideration, Applicants submit that Applicant's Prior Art Fig. 2 (APA) in view of JP No. 9-174909 does not anticipate the present invention, as recited in claims 1, 5 and 12. Applicants, therefore, respectfully request that the rejection of claims 1, 5 and 12, and claims 2-4, 6-11 and 13-17 dependent therefrom under 35 U.S.C. 103(a) be withdrawn.

CONCLUSION

For at least the foregoing reasons, it is believed that all pending claims 1-6 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

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